

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (original): A method for fabricating a thermally-enhanced wafer-level chip scale package, comprising the steps of:

- (1) preparing a semiconductor wafer having a front side and a back side, and which is predefined into a plurality of integrated circuit chips;
- (2) performing a bumping process to bond a plurality of solder bumps on the front side of the semiconductor wafer;
- (3) performing a back-side lapping process to grind away a back-side portion of the semiconductor wafer;
- (4) attaching a thermally-conductive stiffener to the back side of the semiconductor wafer;
- (5) performing a singulation process to cut apart each chip from the semiconductor wafer; and
- (6) performing a flip-chip die bonding process to mount each singulated chip by means of the solder bumps onto a circuited substrate.

Claim 2 (original): The method of claim 1, wherein in said step (4), the thermally-conductive stiffener is attached by means of silver epoxy to the semiconductor wafer.

Claim 3 (original): The method of claim 1, wherein in said step (4), the thermally-conductive stiffener is made of copper.

Claim 4 (original): The method of claim 1, wherein in said step (4), the thermally-conductive stiffener is made of a copper alloy.

Claims 5-8 (canceled)